Adaptive Hysteresis Comparison Control of Load Sharing for Three-Phase Interleaved SCC-LLC Converter

Bo Sheng, Xiang Zhou, Wenbo Liu, Andrew Yurek, Yang Chen, Yan-Fei Liu, *Fellow, IEEE,* and P. C. Sen, *Life Fellow IEEE*

Department of Electrical and Computer Engineering, Queen's University, Kingston, Canada
bo.sheng@queensu.ca, yanfei.liu@queensu.ca

***Abstract*—It is desirable to connect several LLC converters in parallel in high-power and/or high-current applications. However, component tolerance among resonant tank of different phases causes severe unbalanced load sharing, leading to performance degrading. In this paper, full-wave Switch-Controlled Capacitor (SCC) is added into resonant tank to compensate component tolerance and to achieve load sharing. An adaptive hysteresis comparison control scheme is proposed to adjust SCC angle α for current sharing. The proposed control strategy only occupies few digital controller resources; thus, low-cost Micro-Controller Unit (MCU) can be used. Experimental results of a 250V - 430V input, 14V/260A/3.6kW output, three-phase interleaved SCC-LLC EV DC-DC converter demonstrate the effectiveness and feasibility of the proposed method.**

Keywords— LLC converter, Load sharing, Switched-Controlled Capacitor (SCC), Adaptive hysteresis comparison control

I. INTRODUCTION

With advancements of power conversion technology and power electronics devices, high efficiency and high power density become a major challenge for front-end DC/DC converters. LLC resonant converter has been widely accepted in recent years by providing both high efficiency and high power density for numerous applications, such as servers, flat panel TVs, and LED lightings [1, 2]. However, LLC converter experiences limitations when works at heavy load condition. The major difficulty is the high conduction loss on secondary side synchronous rectifiers (SRs).

To operate LLC converter in high-power high-current applications, interleaving technique could be used. With interleaving, total output current is split into different phases. Thus, the I^2R loss will be reduced to I^2R/N if N phases are interleaved. When interleaved, all phases operate at same switching frequency. While the voltage gain of each phase at same switching frequency is different from each other if taking resonant tank tolerances into consideration. Different voltage gains cause output current unbalance, which will degrade the system performance severely. Recently, several solutions have been proposed to achieve current sharing, including current-controlled inductor [3], star connection of transformer primary side windings [4], and turn-on timing control for secondary side switches [5]. However, all these methods have limitations. Particularly, [3] needs to add extra inductors which are not only large but costly, [4] is only suitable for three-phase LLC interleaving topology, and [5] makes the operation of secondary side switches complicated. Besides, the current-rating of rectified diode on secondary side restricts the maximum output current. In [6] and [7], the authors used passive impedance matching to achieve current sharing among multiple phases. Resonant inductors or capacitors are connected in parallel to form common inductor or common capacitor structures. However, phase shift and phase shedding among different phases cannot be obtained by using this method.

The concept of Switch-Controlled Capacitor (SCC) was introduced in [8]. It provides a simple solution for interleaving, load sharing and phase shedding. Both half-wave SCC and full-wave SCC have been successfully applied in two-phase LLC converter to achieve interleaving and load sharing [9, 10]. The authors either combined fixed switching frequency with full-wave SCC or variable switching frequency with half-wave SCC. However, the first solution limited the voltage gain variation range, which made the circuit only work in a narrow input and output range. The second solution needed extra logic circuit to prevent SCC MOSEFT body diode from conducting. Moreover, since only one phase was designed with SCC, it may lose current sharing ability if the phase with SCC carries higher current than that of the phase without SCC.

In this paper, full-wave SCC is applied on each phase in a three-phase LLC converter. The topology of three-phase interleaved full-wave SCC-LLC converter is shown in Fig. 1. Ideally, the 260A full load will be equally distributed into three phases. Thus, single-phase converter is designed to carry 1/3 of the total load which is 86A. Due to the existing of SCC on each phase, current sharing can be achieved no matter which phase could potentially carry the highest/lowest current. Frequency modulation is used to regulate output voltage. An adaptive hysteresis comparison control scheme is proposed to control SCC MOSFETs. The proposed control strategy can be integrated into a cost-effective Micro-Controller Unit (MCU). Section II discussed the operation principle of half-wave and full-wave SCC. Section III analyzed the load sharing characteristic of LLC converter. Section IV explained the details of the proposed control method. Experimental results and a conclusion are provided in section V and section VI.

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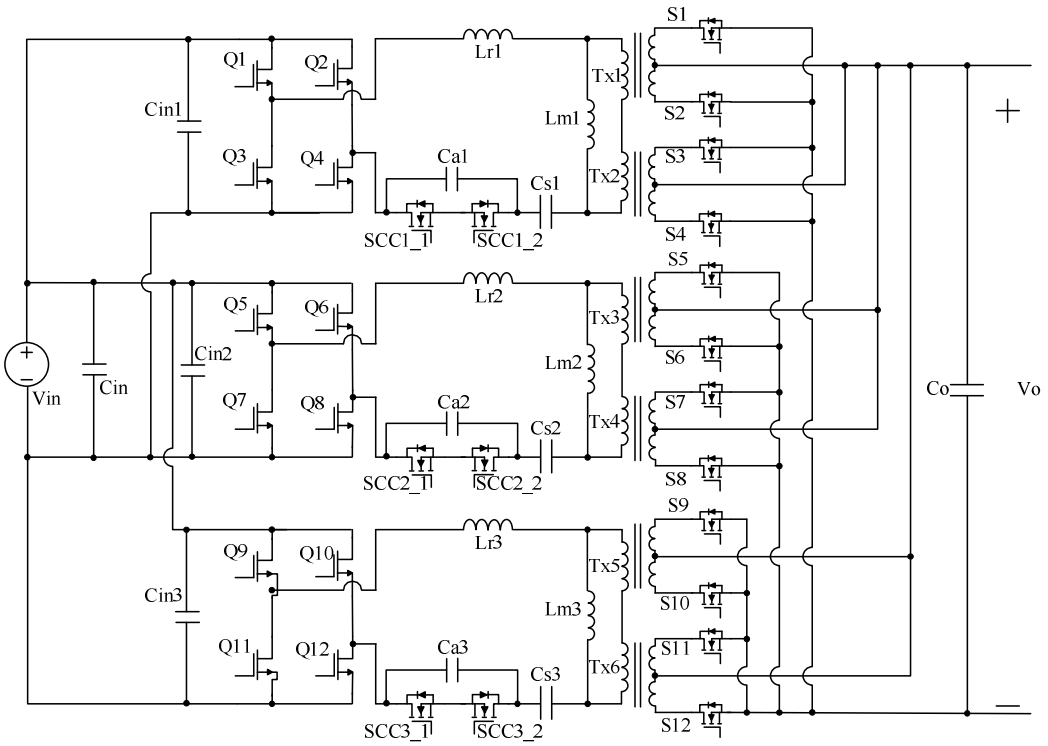


Fig. 1. Three-phase interleaved full wave SCC-LLC resonant converter

II. Operation Principle of SCC Circuit

Through turning on/off of SCC MOSFET, both half-wave and full-wave SCC circuits can be used to adjust the equivalent resonant capacitance in LLC converter. This section discusses the operation principle of both SCC circuits.

A. Half-wave SCC circuit

Fig. 2 shows the schematic of a half-wave SCC circuit. It consists a capacitor in parallel with a MOSFET. Fig. 3 presents the operation waveform of the half-wave SCC circuit. By connecting the SCC capacitor C_a in and out of the resonant tank, the equivalent resonant capacitance could be modulated. The operation principle of half-wave SCC is described as follows.

Assuming a sinusoidal current I_{AB} is flowing through the SCC circuit, the current zero-crossing points are at angle 0, π, 2π, …. etc. For a positive half cycle, SCC1 is turned off at angle 2nπ+α, or α degree after the zero-crossing points (from negative to positive) of the current. After SCC1 is turned off, the current flows from A to B via C_a and charges the capacitor until the next current zero-crossing point at (2n+1)π. Then, the current reverse direction, and begins to discharge C_a. After C_a is fully discharged, the negative current is about to flow from B to A via the body diode of SCC1. SCC1 is turned on as soon as the C_a voltage drops to zero. Thus, ZVS turn-on is achieved for SCC1. Moreover, its body diode is not conducted. SCC1 remains on for the rest of the cycle and turns off again at angle (2n+2)π+α. The delay angle α is defined from the positive current zero-crossing point to the SCC1 turn-off point. Its variation range is from 0° to 180°. Since a large capacitor C_a (nF) is connected in parallel with SCC1, the voltage V_{Ca} rises slowly after SCC1 is turned off. Therefore, ZVS turn-off is also achieved.

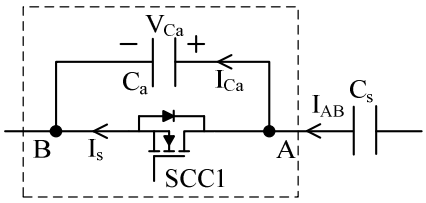


Fig. 2. Schematic of the half-wave SCC circuit

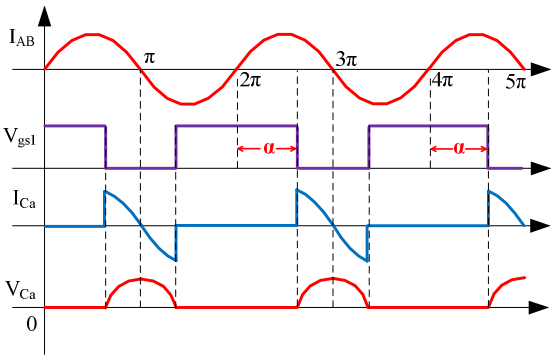


Fig. 3. Waveform of the half-wave SCC circuit

Considering the fundamental component in V_{Ca} and I_{AB} Fourier series, the equivalent capacitance of the half-wave SCC circuit can be derived in (1) [8, 9].

$$C_{SC} = \frac{2C_a}{2-(2\alpha - sin(2\alpha))/\pi} \quad (1)$$

For LLC converter, the equivalent resonant capacitor becomes the series connection of the half-wave SCC and the series resonant capacitor C_s, as shown in Fig. 2. The equivalent resonant capacitance is calculated in (2).

$$C_r = \frac{C_{sc}C_s}{C_{sc}+C_s} \quad (2)$$

Substituting (1) into (2), the equivalent resonant capacitance can be rewritten in (3).

$$C_r = \frac{2\pi C_a C_s}{2\pi(C_a+C_s) - 2\alpha C_s + sin(2\alpha)C_s} \quad (3)$$

When α = 0°, SCC1 and its body diode keep OFF all the time. Current I_{AB} flows through capacitor C_a. The equivalent resonant capacitance is at the minimum value which is equal to C_s and C_a connected in series. When α = 180°, SCC1 keeps ON all the time. The SCC capacitor is short circuit, which makes the equivalent resonant capacitance equal to its maximum value C_s.

As described before, half-wave SCC circuit only modulates resonant capacitance in positive half cycle, which causes asymmetrical resonant current in positive and negative half cycles. Thus, the energy transferred to output side in both half cycles are different, which is not desirable for LLC converter.

B. Full-wave SCC circuit

To achieve symmetrical resonant current, full-wave SCC circuit can be applied. The structure of a full-wave SCC circuit is shown in Fig. 4. The circuit consists a capacitor and two MOSFETs with back-to-back configuration. The control angle α for full-wave SCC changes from 90° to 180°. Fig. 5 shows the corresponding operation waveform. The control scheme can be described as follows.

For a positive half cycle, SCC1 is turned off at angle 2nπ+α, or α degree after the zero-crossing points (from negative to positive) of the current. After SCC1 is turned off, current I_{AB} flows from A to B via C_a. Due to the large capacitance of C_a, the voltage V_{Ca} increases slowly, leading to ZVS turn-off for SCC1. The current keeps charging the capacitor until next current zero-crossing point at (2n+1)π. Then, the current reverses direction, and begins to discharge C_a. After C_a is fully discharged, the negative current is about to flow from B to A via the body diode of SCC1. To achieve ZVS turn-on and prevent the body diode from conducting, SCC1 is turned on as soon as the capacitor voltage drops to zero. It remains on for the rest of cycle and turns off again at angle (2n+2)π+α. Following the same procedure, SCC2 controls the negative half cycle. It is turned off at angle (2n+1)π+α, or α degree after the zero-crossing points (from positive to negative) of the current. When capacitor voltage V_{Ca} discharges to zero, SCC2 is turned on with ZVS. Besides, due to the large capacitance of C_a, ZVS turn-off is also achieved for SCC2.

It can be observed from Fig. 5 that current I_{AB} flows through SCC1 and SCC2, if both switches are ON at the same time, otherwise, it flows via C_a to charge and discharge it.

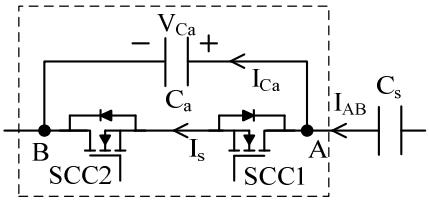


Fig. 4. Structure of the full-wave SCC circuit

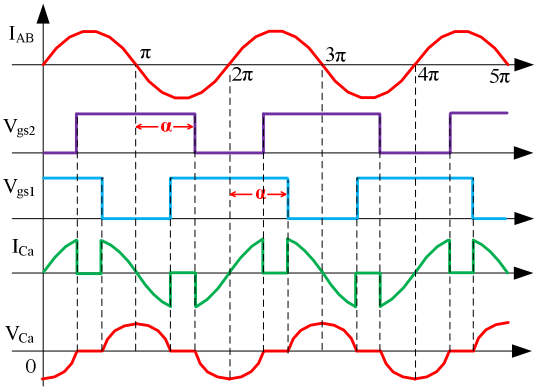


Fig. 5. Waveform of the full-wave SCC circuit

Considering the fundamental components in V_{Ca} and I_{AB} Fourier series, the equivalent capacitance of full-wave SCC, C_{SC} can be calculated as a function of delay angle α, shown in (4).

$$C_{SC} = \frac{C_a}{2-(2\alpha - sin(2\alpha))/\pi} \quad (4)$$

The equivalent resonant capacitance can be rewritten in (5).

$$C_r = \frac{\pi C_a C_s}{\pi C_a + 2\pi C_s - 2\alpha C_s + sin(2\alpha)C_s} \quad (5)$$

When α = 90°, SCC1 and SCC2 are not ON at the same time. Current I_{AB} always flows through capacitor C_a, making capacitor C_a fully connected into the circuit. The equivalent resonant capacitance is at the minimum value which is equal to C_s and C_a connected in series. When α = 180°, SCC1 and SCC2 are always ON, and C_a is short circuit by these two MOSFETs. The equivalent resonant capacitance is at its maximum value C_s.

Fig. 6 shows the ratio of equivalent resonant capacitor C_r over series resonant capacitor C_s with respect to SCC angle α. In this example, C_s is 3.4nF, and C_a is 10nF. From Fig. 6, the ratio C_r/C_s for half-wave SCC is changing from 0.75 to 1 over entire delay angle α variation range from 0° to 180°. Moreover, full-wave SCC has the same C_r modulation capacity compared to half-wave SCC. But, the delay angle α varies from 90° to 180°.

To sum up, both half-wave and full-wave SCC achieve ZVS operation during turn-on and turn-off process. The body diode of SCC MOSFET is not conducted. The power loss on SCC circuit is only the MOSFET conduction loss. Besides, they have the same capacitance modulation range. Furthermore, both SCC circuits compensate component tolerance through decreasing equivalent resonant capacitance. However, compared to half-

wave SCC, full-wave SCC is preferred for LLC converter due to the symmetrical modulation in both positive and negative half cycles. This paper will focus on applying full-wave SCC circuit into LLC converter.

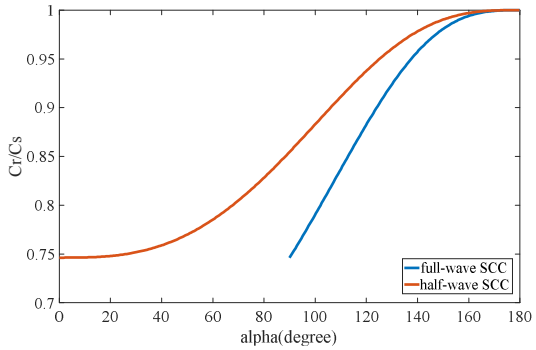


Fig. 6. Capacitance ratio of C_r over C_s with respect angle α at C_s = 3.4nF, C_a = 10nF

III. Load Sharing Characteristic of LLC Converter

Due to component tolerances, the resonant frequencies of interleaved phases are slightly different from each other, which will cause different voltage gains at same switching frequency. The voltage gain of LLC converter in boost mode can be derived using time-domain method [11, 12]. The voltage gain function is expressed in (6).

$$\frac{V_o}{V_{in}} = -\frac{2}{n}\frac{1}{\frac{Z_o\omega_o}{4n^2 f_{sw} R}(cos\beta - 1) + \frac{\pi Z_1}{2L_m\omega_o} sin\beta - (cos\beta + 1)} \tag{6}$$

All definitions are given in (7).

$$Z_o = \sqrt{\frac{L_r}{C_s}},\ Z_1 = \sqrt{\frac{L_r + L_m}{C_s}},\ \omega_o = \frac{1}{\sqrt{L_r C_s}},\ \omega_1 = \frac{1}{\sqrt{(L_r + L_m)C_s}}$$

$$\beta = \pi\omega_1\left(\frac{1}{2\pi f_{sw}} - \frac{1}{\omega_o}\right) \tag{7}$$

Where, f_{sw} is switching frequency in hertz, and ω_o is the resonant frequency in radians.

A set of voltage gain curves are obtained based on (6) and plotted in Fig. 7. The specification is: V_{in} = 380V, V_o = 14V, and I_o = 86A. The transformer turns ratio is 44 : 1. The nominal values of resonant components L_r, L_m, and C_r are 25uH, 125uH, and 3.4nF, respectively. Moreover, +5% tolerance is assumed on L_r, L_m, and C_r for the first phase. 0% and -5% tolerances are assumed on L_r, L_m, and C_r for the second phase and the third phase, respectively.

From Fig. 7, different component tolerance causes different voltage gains at same switching frequency. Taking 340kHz as an example, the first phase with -5% tolerance has the highest voltage gain, which is around 1.54. It is reduced to 1.45 with 0% tolerance. The third phase with +5% tolerance has the lowest voltage gain, which is 1.39 at 340kHz.

As mentioned before, when interleaved, all three phases operate at same switching frequency. Furthermore, the input voltage and output voltage are the same for three phases due to the input-parallel and output-parallel structure. Thus, same voltage gain at same switching frequency is a prerequisite for interleaving. When three phases are connected in parallel, the first phase will carry a heavier load to reduce its voltage gain, and the third phase will output a lighter load to increase its voltage gain. Therefore, severe load unbalance will happen.

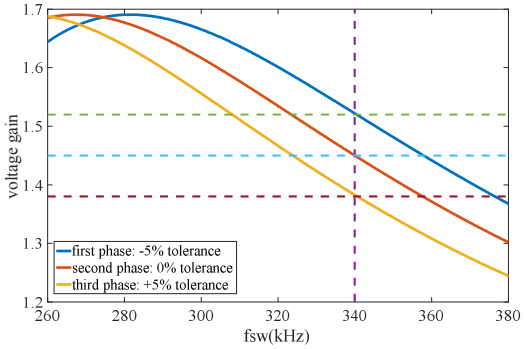


Fig. 7. Voltage gains of LLC converter at 380V input, 14V/86A output

Based on (6), the output current can be calculated in (8).

$$I_o = \frac{4n^2 f_{sw} V_o}{Z_o\omega_o(cos\beta - 1)}\left(cos\beta + 1 - \frac{2V_{in}}{nV_o} - \frac{\pi Z_1}{2L_m\omega_o} sin\beta\right) \tag{8}$$

Fig. 8 shows the output current versus switching frequency at 380V input, 14V output. The peak output current obtained by mathematic calculation is the theoretical maximum capacity of such resonant tank. At 340kHz, the output current for three phases are 63A, 26A and 0A, respectively. The first phase with -5% tolerance carries 63A load. On the other hand, the third phase with +5% tolerance carries 0A load. This is consistent with the results analyzed from voltage gain point of view. In summary, there is no current sharing among three phases when component tolerance is considered.

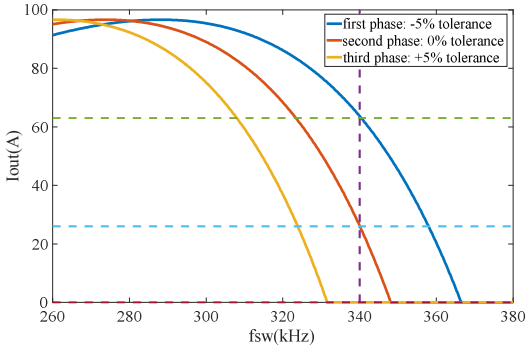


Fig. 8. Output current of LLC converter at 380V input, 14V output

To compensate component tolerance and achieve load sharing, full-wave SCC circuit can be applied into the resonant tank. By controlling the delay angle α, the equivalent resonant capacitor C_r is adjusted so that the voltage gain could be modulated to match with each other. Finally, current sharing could be obtained. With SCC compensation, the output current can be recalculated in (9).

$$I_o(f_{sw},\alpha) = \frac{4n^2 f_{sw} C_r(\alpha) V_o}{\cos\beta - 1}\left(\cos\beta + 1 - \frac{2V_{in}}{nV_o} - \frac{\pi}{2}\sqrt{\frac{1}{L_m}\left(\frac{1}{L_r}+\frac{1}{L_m}\right)}\sin\beta\right) \quad (9)$$

Where, $C_r(\alpha)$ is a function of delay angle α. For full-wave SCC, C_r is defined in (5).

Defining the actual values of resonant components for three phases are L_{r1}, L_{m1}, C_{s1}, C_{a1}, L_{r2}, L_{m2}, C_{s2}, C_{a2}, and L_{r3}, L_{m3}, C_{s3}, C_{a3}, respectively. Tolerances on resonant components are included. The output currents of all three phases are expressed in (10), (11) and (12), respectively.

$$I_{o1}(f_{sw},\alpha_1) = \frac{4n^2 f_{sw} C_{r1}(\alpha_1) V_o}{\cos\beta - 1}\left(\cos\beta + 1 - \frac{2V_{in}}{nV_o} - \frac{\pi}{2}\sqrt{\frac{1}{L_{m1}}\left(\frac{1}{L_{r1}}+\frac{1}{L_{m1}}\right)}\sin\beta\right) \quad (10)$$

$$I_{o2}(f_{sw},\alpha_2) = \frac{4n^2 f_{sw} C_{r2}(\alpha_2) V_o}{\cos\beta - 1}\left(\cos\beta + 1 - \frac{2V_{in}}{nV_o} - \frac{\pi}{2}\sqrt{\frac{1}{L_{m2}}\left(\frac{1}{L_{r2}}+\frac{1}{L_{m2}}\right)}\sin\beta\right) \quad (11)$$

$$I_{o3}(f_{sw},\alpha_3) = \frac{4n^2 f_{sw} C_{r3}(\alpha_3) V_o}{\cos\beta - 1}\left(\cos\beta + 1 - \frac{2V_{in}}{nV_o} - \frac{\pi}{2}\sqrt{\frac{1}{L_{m3}}\left(\frac{1}{L_{r3}}+\frac{1}{L_{m3}}\right)}\sin\beta\right) \quad (12)$$

With a good SCC compensation, the output currents of three phases will be the same. Thus, the following relationship can be built in (13).

$$\begin{aligned} I_{o1}(f_{sw},\alpha_1) &= I_{o2}(f_{sw},\alpha_2) \\ I_{o1}(f_{sw},\alpha_1) &= I_{o3}(f_{sw},\alpha_3) \\ I_{o2}(f_{sw},\alpha_2) &= I_{o3}(f_{sw},\alpha_3) \end{aligned} \quad (13)$$

There are four unknown parameters in three equations, which are switching frequency f_{sw}, and delay angle α_1, α_2, and α_3. In theory, multiple combinations of f_{sw} and delay angle α can be solved to meet current sharing requirement. To solve (13), either f_{sw} or one of the delay angle α should be assigned to a given value. Since frequency modulation is used to regulate output voltage, wide variation range is expected for f_{sw}. SCC angle α is tuned to compensate component tolerance, which has smaller impact on the normal operation of LLC converter. It is reasonable to set one of delay angle α to a given value.

Note that SCC only decreases the equivalent resonant capacitance and increases the resonant frequency. The increasing on resonant frequency shifts the voltage gain curve to the right, which increases the voltage gain at same switching frequency. To maintain same voltage gain, the output current of that phase will be increased. Therefore, when angle α decreases, the output current increases. Besides, larger angle α reduces capacitor C_a charging time, leading to lower voltage amplitude across it. Thus, lower voltage rating MOSFET can be used, whose turn-on resistance is usually also lower. It is a good choice to set the delay angle α to its maximum for the phase that carries the highest load current; then, reducing delay angle α of other two phases to increase their output current to match with the highest load current phase.

In the example, the first phase carries the highest output current. Setting α_1 to 180°, equation (13) can be solved with f_{sw} = 340kHz, α_2 = 123°, α_3 = 103°, and $I_{o1} = I_{o2} = I_{o3}$ = 63A. Fig. 9 shows the relationship of output current versus SCC angle α. To output 63A load, α_2 and α_3 are reduced to 123° and 103°. With SCC compensation, the voltage gain curves at 380V input, 14V/63A output are drawn in Fig. 10. Three gain curves are intersected at 340kHz with a voltage gain of 1.54, which means that three phases have the same voltage gain at same switching frequency with same load condition. Thus, current sharing could be guaranteed.

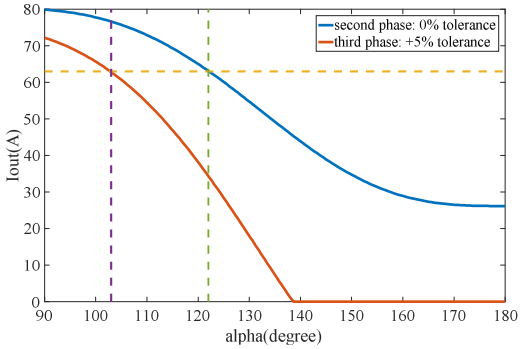


Fig. 9. Output current versus angle α at 380V input, 14V output and 340kHz frequency

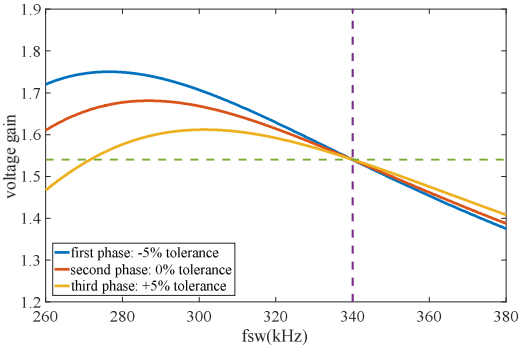
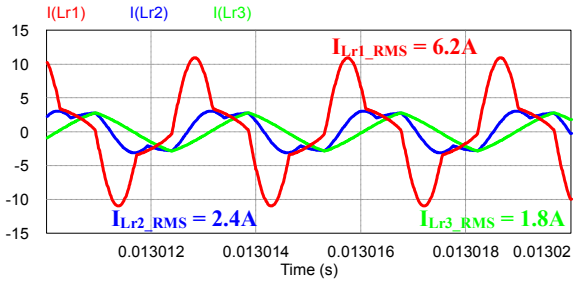


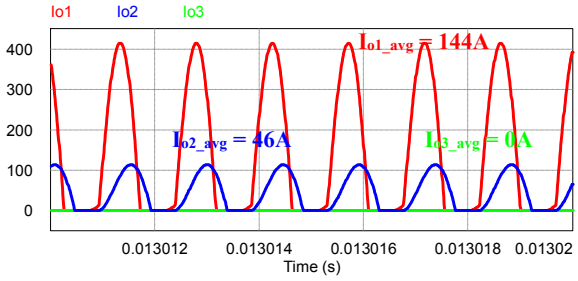
Fig. 10. Voltage gains of LLC converter with SCC compensation

The simulation model of three-phase LLC converter has been built and studied by using PSIM with same parameters in mathematical analysis. -5%, 0% and +5% tolerance have been assumed on resonant components for the first phase, the second phase and the third phase, respectively. Fig. 11 shows the simulation waveform of resonant current and secondary side rectified current at 380V input, 14V output, 340kHz frequency. The total output current is 190A without SCC current sharing. It

can be observed from Fig.11 (b) that the average load current for each phase are 144A, 46A and 0A, respectively. There is no current sharing among three phases. Besides, the first phase carries the highest load current than the other two phases.



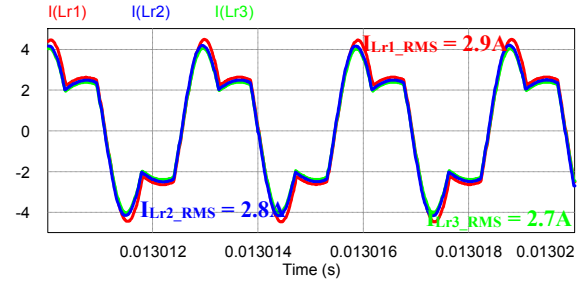
(a) resonant current (I_{Lr1}: -5% tolerance, I_{Lr2}: 0% tolerance, I_{Lr3}: +5% tolerance)



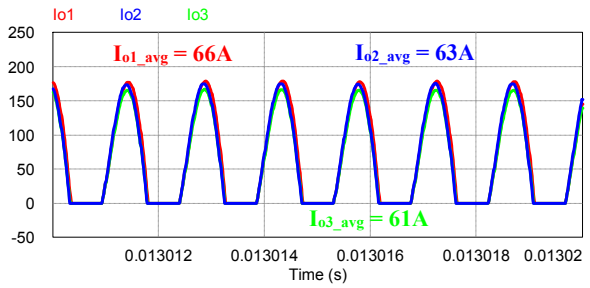
(b) rectified current (I_{o1}: -5% tolerance, I_{o2}: 0% tolerance, I_{o3}: +5% tolerance)

Fig. 11. Simulated waveform at 380V input, 14V output and 340kHz frequency without SCC compensation

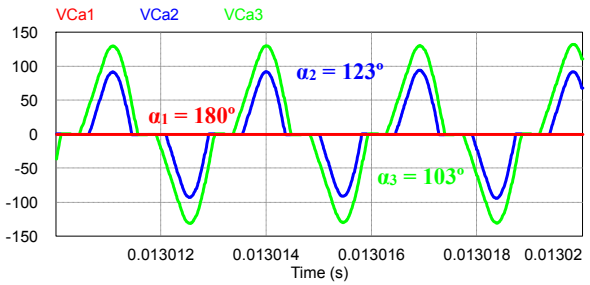
Fig. 12 also shows the simulation results at 380V input, 14V output, 340kHz frequency. The total output load is 190A with SCC current sharing. Based on previous mathematical analysis, angle α_1 of the first phase is set to 180°. Angle α_2 and α_3 are set to 123° and 103°. From Fig. 12 (b), three phases carry almost the same amount of load, which is around 63A. The simulation result demonstrated that SCC circuit can help achieve current sharing. However, the total output load is not exactly divided among three phases, the third phase still carries the lowest output current. This is because the developed mathematical model is relatively simpler and less accurate compared to simulation model. If closed loop is implemented, the current sharing performance can be improved. Fig. 12 (c) shows the simulated waveform of three phases SCC capacitor voltage. The first phase SCC capacitor voltage keeps at 0V. This is because angle α_1 is set to 180°; the capacitor is short circuited by SCC MOSFETs.



(a) resonant current (I_{Lr1}: -5% tolerance, I_{Lr2}: 0% tolerance, I_{Lr3}: +5% tolerance)



(b) rectified current (Io1: -5% tolerance, Io2: 0% tolerance, Io3: +5% tolerance)



(c) SCC capacitor voltage (V_{Ca1}: -5% tolerance, V_{Ca2}: 0% tolerance, V_{Ca3}: +5% tolerance)

Fig. 12. Simulated waveform at 380V input, 14V output and 340kHz frequency with SCC compensation

IV. Adaptive Current Sharing Control Strategy

Among digital controllers, the cost-effective MCU is preferred in industrial applications. In this work, two Microchip DSCs dsPIC33FJ32GS610 are used to implement the proposed control scheme. The voltage loop is implemented in secondary side MCU by using conventional PI control. Frequency modulation is performed to regulate output voltage. The current loop is implemented in primary side MCU. An adaptive hysteresis comparison control scheme is proposed to adjust SCC angle α.

It is desirable to achieve largest angle α for the phase that carries the highest load current so that the voltage rating of SCC MOSFET can be reduced. In addition, when delay angle α is reduced, the output current of that phase will be increased, and vice versa. The proposed SCC angle α tuning process is described as follows.

At start up, three phases angle α are set to the maximum value. The difference among three phases output current is large. Based on energy balancing, all three phases' input current are sampled and compared to estimate output current sharing performance. Of all three phases, there is one phase which produces the highest current; and there is another phase which produces the lowest current. Delay angle α is tuned by Δα degree every step based on the comparison result. The controller keeps checking angle α of the highest current phase. If the angle α is smaller than its maximum value, the controller increases the angle α to decrease its output current at first. Until the angle α arrives its maximum value, the controller starts to decrease angle α of the lowest current phase to increase its output current. After several cycles, new relationship among three phases' input

current will be built, and the controller adjusts angle α based on new comparison result. The angle α is tuned step-by-step to eliminate the difference of three-phase input current. Finally, the total output current will be distributed into three phases equally. Fig. 13 shows the flowchart of the proposed current sharing strategy. To filter out unexpected current sensing noise, hysteresis is added into the current loop. Only if the comparison result of three phases input current keeps constant for consecutive several times, angle α of the corresponding phase will be updated then; otherwise, angle α will keep unchanged. Thanks to the existing of SCC on each phase, current sharing could always be achieved no matter which phase carries the highest or the smallest current.

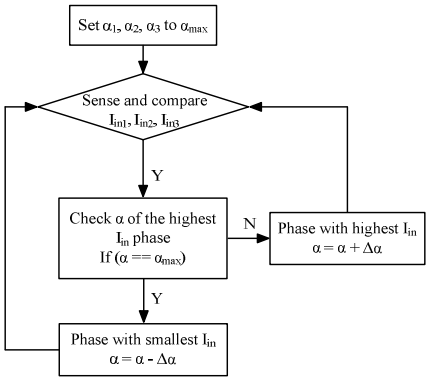


Fig. 13. Control flowchart of the proposed current sharing strategy

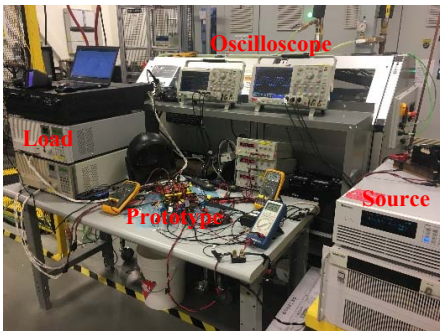
To avoid oscillation and eliminate the interference between two loops, current loop is designed much slower than voltage loop. By doing so, SCC angle α tuning is always performed with stabilized and constant output voltage. Besides, current loop will not interfere the operation of voltage loop, which is the highest priority for the LLC converter to work correctly.

PWM module in MCU is used to generate gate single for SCC MOSFET. The PWM signal is synchronized with the zero-crossing points of resonant current of corresponding phase. A current transformer (CT) and a comparator are applied to sense the resonant current zero-crossing point. Then, the output of the comparator is transmitted to MCU as an external interrupt (INT) to reset SCC PWM signal.

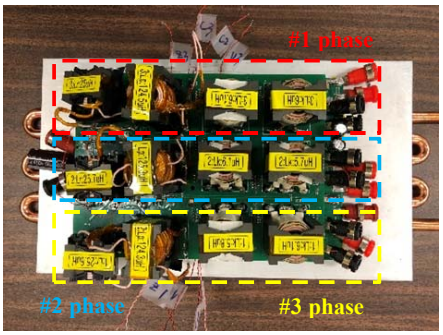
V. Experimental Results

To verify the effectiveness of the proposed control strategy, a 250V – 430V input 14V/260A output three-phase SCC-LLC EV DC-DC converter was built and tested. The photo of the testing bench and the developed prototype are shown in Fig. 14. The prototype size is 185mm × 135mm × 48mm, with a power density of 3kW/L. The parameters of developed converter are given in Table I.

Fig. 15 shows the waveform of single-phase converter at 380V input, 14V/90A output. The SCC angle α is kept at 130°. It can be observed from Fig. 15 that SCC MOSFETs are turned on as soon as the capacitor voltage is discharged to zero. ZVS turn-on is achieved, and the body diode does not conduct. Moreover, the SCC capacitor voltage rises slowly after SCC MOSFETs are turned off. Thus, ZVS turn-off is also achieved.



(a) Testing bench



(b) Developed prototype

Fig. 14. Testing bench and developed prototype of the three-phase SCC-LLC EV DC-DC converter

TABLE I. Parameters of Three-Phase SCC-LLC Converter

Circuit Parameters	
Transformer	N = 44, PQ35/35 core
Parallel inductor	L_{m1} = 125.5μH, L_{m2} = 124.2μH, L_{m3} = 127.2μH, PQ35/35 core
Series inductor	L_{r1} = 26.1μH, L_{r2} = 25.7μH, L_{r3} = 26.1μH, PQ32/20 core
Series capacitor	C1808C681JGGAC7800 2KV, 680pF × 5 (per phase)
SCC capacitor	C2012NP02W472J125AA, 450V, 4700pF × 3 (per phase)
Primary side GaNs	GS66508B (650V, 30A) × 4 (per phase)
Secondary side SRs	TPHR8504PL (40V, 150A) × 12 (per phase)
SCC MOSFETs	IPB200N25N3 (250V, 64A) × 2 (per phase)
Output capacitor	C3216JB1E336M160AC, 25V, 33μF × 10 (per phase)
MCU	DSPIC33FJ32GS610 × 2

Fig. 16 shows the resonant current and the SCC capacitor voltage at 380V input, 14A/260A output. The maximum α is set to 140°. From Fig. 16, the second phase angle α_2 is at the maximum value. Angle α_1 and α_3 are reduced to 123 and 115° to achieve current sharing. The RMS current of three phases are 3.86A, 3.95A and 4A. Good current sharing performance is obtained. In addition, 0°, 60° and 120° phase shift is implemented among three phases to mitigate output voltage ripple.

Fig. 17 shows the measured efficiencies of the developed prototype at 250V input, 330V input and 380V input, respectively. Due to good current sharing performance among three phases, high efficiency is achieved. Particularly, a peak

efficiency of 96.7% and a full load efficiency of 95.8% have been achieved at 380V input, 14V output.

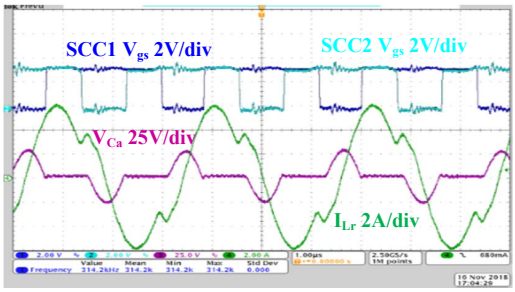
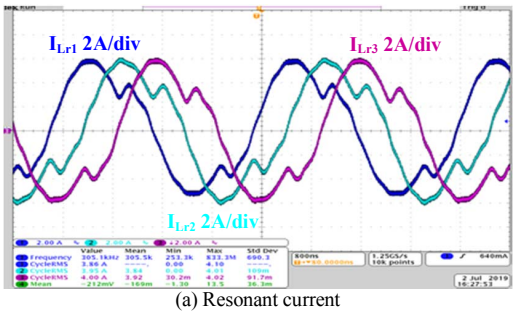
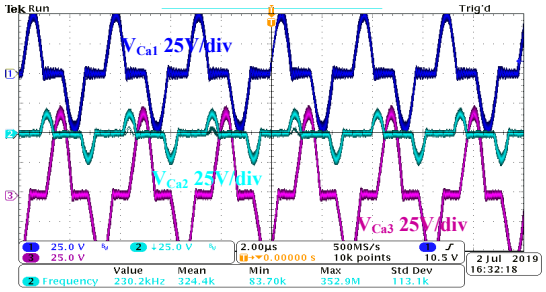


Fig. 15. Waveform of single-phase SCC-LLC converter at 380V input, 14V/90A output



(a) Resonant current



(b) SCC capacitor voltage

Fig. 16. Waveform of three-phase SCC-LLC converter at 380V input, 14V/260A output

VI. Conclusion

In this paper, full-wave SCC circuit is applied into a three-phase LLC converter. The operation principle of SCC circuit is discussed. Thanks to the control scheme, both ZVS turn-on and turn-off are obtained for SCC MOSFET. Moreover, the body diode of SCC MOSFET is not conducting. The load sharing characteristic of LLC converter without and with SCC is investigated through mathematical analysis and simulation studies. An adaptive current sharing control strategy is proposed to adjust SCC angle α. Experimental results of a 250V – 430V input, 14V/260A output, three-phase SCC-LLC EV DC-DC converter demonstrate that excellent current sharing performance is achieved with high efficiency and high power density.

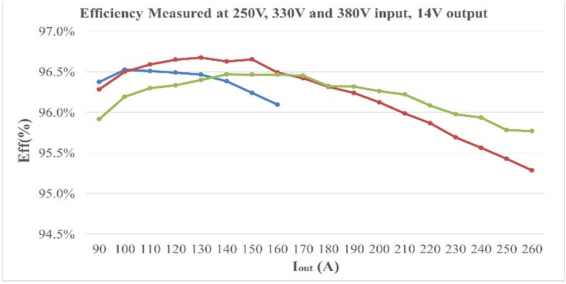


Fig. 17. Measured efficiencies of developed prototype at 250V, 330V and 380V input

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